

REMARKS

The specification has been amended to replace the attorney docket number with the corresponding U.S. patent application serial number.

Claim 1 has been amended to incorporate the features of Claim 2, which has accordingly been canceled without prejudice.

Claims 3, 4, and 5, which previously depended from Claim 2, have been amended to depend from Claim 1. Claims 6 and 8 have been amended to correct obvious typographical errors.

The headings below are numbered to correspond with the heading numbering used by the Examiner in the Office Action.

1/2) Claim 4 satisfies 35 U.S.C. 112, second paragraph.

The Examiner states:

The term "sufficiently" in claim 4 is a relative term, which renders the claim indefinite. **The term "sufficiently" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree,** and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. If applicants intends any particular optical transmittance, it must be clearly recited. (Office Action, page 2, emphasis added.)

The Examiner's statement is respectfully traversed. Initially, Applicants note that Claim 4 provides a standard for the term "sufficiently". Specifically, Claim 4 recites: "wherein said wafer support is **sufficiently transparent to allow said first intersection to be optically recognized through said wafer support**", emphasis added.

Further, Applicants' specification recites:

Generally, wafer support 204 is sufficiently transparent to allow optical recognition, e.g., by the operator or alignment system, of scribe grid 116 through wafer support 204. (Page 7, lines 24-27.)

Accordingly, Applicants respectively submit that one of skill in the art would understand what is being claimed in Claim 4 when read in light of the specification. Accordingly, Claim 4 satisfies 35 U.S.C. 112, second paragraph.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

3/4) Claims 1, 7, 9-13 are novel over Wojnarowski.

At page 4 of the Office Action, the Examiner admits that:

Wojnarowsky fail to teach coupling a front-side surface of a wafer to an interior surface of a transparent wafer support; ... (emphasis added.)

Claim 1 has been amended and now recites a method comprising:

coupling a wafer support to a first surface of a substrate;

aligning a drilling device at a first intersection of a first scribe line and a second scribe line coupled to said first surface of said substrate; and

drilling through said substrate at said first intersection with said drilling device from said first surface to a second surface of said substrate to form an alignment mark. (Emphasis added.)

For at least the above reasons, Claim 1 is allowable over Wojnarowski. Claims 7, 9-13, which depend from Claim 1, are allowable for at least the same reasons as Claim 1.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

5/6) Claims 3-6, 14-21 are patentable over Wojnarowski in view of Roberts, Jr. et al.

The features of Claim 2 have been incorporated into Claim 1. Thus the rejection of Claim 2 shall be discussed as applied to Claim 1.

The Examiner admits:

Wojnarowsky fail to teach coupling a front-side surface of a wafer to an interior surface of a transparent wafer support; optically recognizing a scribe grid coupled to said front-side surface of said wafer through said wafer support, wherein said support protects the front surface of said substrate; and washing said substrate to remove contaminants generated during said cutting. (Office Action, page 4, emphasis added.)

To cure this glaring deficiency of Wojnarowski, the Examiner cites Roberts, Jr. et al. Specifically, the Examiner states:

... Roberts Jr., et al. (Figs. 2-5) in a related method to singularize a semiconductor wafer teach coupling a front-side surface of a wafer (32) to an interior surface of a transparent wafer support (26); **optically aligning the wafer through said wafer support**, wherein said support protects the front surface of said substrate; and washing said substrate to remove contaminants generated during said cutting ... (Office Action, page 4, emphasis added.)

The Examiner's statement that Roberts, Jr. et al. teaches "optically aligning the wafer **through said wafer support**" is respectfully traversed. Roberts, Jr. et al. teaches that the "wafer support" includes alignment marks formed in an exposed region of the "wafer support", which extends beyond the wafer, and that these alignment marks are used to align the wafer. Since the "wafer support" of Roberts, Jr. et al. already includes alignment marks, one of skill in the art would have no motivation to provide additional alignment marks as asserted by the Examiner. Accordingly, one of skill in the art would have no motivation to combine the teachings of Roberts, Jr. et al. with the teachings of Wojnarowski as asserted by the Examiner.

Specifically, referring to FIG. 4, Roberts, Jr. et al. teaches:

An additional set of alignment holes 30a and 30b are punched in the film **such they will be beyond the perimeter of the wafer** when the wafer is adhered to the film. (Col. 6, lines 36-38, emphasis added.)

Further, referring to FIG. 5, Roberts, Jr. et al. teaches:

... Holes 30a and 30b, however, are exposed beyond the perimeter 35 of the wafer. ... The sawing station comprises a camera which obtains the image of the film frame assembly and determines the position of holes 30a and 30b. **The sawing station is programmed with a map of the wafer indicating the relative position of each street relative to the lines defined by holes 30a and 30b.** (Col. 8, lines 17-29, emphasis added.)

Further, Wojnarowski teaches that the front-side surface of the wafer must be processed. Since applying a "wafer support" to this front-side surface would defeat the ability to process the front-side surface, combining Wojnarowski with Roberts, Jr. et al. would result in an inoperative assembly and thus one of skill in the art would not make such a combination. Specifically, Wojnarowski teaches:

Referring next to FIG. 3, an insulating coating 54 is formed on all exposed surfaces of wafer 30, including **top 32, bottom 34 and within holes 50.** ... With reference to FIG. 4, openings 56 are formed in insulating layer 54 to provide access to **top** interconnection pads 40. ... With reference to FIG. 5, wafer 30 ... [is] backspattered and metallized on **both sides**, forming metallization 60. ... A resist (not shown) can be applied to wafer 30, **covering all surfaces.** ... As shown in FIG. 6, the resist is developed and all excess metal removed, leaving patterned metal 62 by which **top** wafer pads 40 are electrically relocated to metal pads 64 on the bottom 34 of wafer 30. (Col. 7, lines 16-53, emphasis added.)

For at least the above reasons, Wojnarowski in view of Roberts Jr., et al. does not teach or suggest a method comprising:

coupling a wafer support to a first surface of a substrate;

aligning a drilling device at a first intersection of a first scribe line and a second scribe line coupled to said first surface of said substrate; and

drilling through said substrate at said first intersection with said drilling device from said first surface to a second surface of said substrate to form an alignment mark,

as recited in amended Claim 1, emphasis added. Accordingly, Claim 1 is allowable. Claims 3-6, which depend from Claim 1, are allowable for at least the same reasons as Claim 1.

Claims 14 and 20 are allowable for reasons similar to Claim 1. Claims 15-19, which depend from Claim 14, are allowable for at least the same reasons as Claim 14.

Further, Claim 21 recites a method comprising:

coupling a front-side surface of a wafer to a wafer support, a first scribe line and a second scribe line being coupled to said front-side surface;

optically recognizing an intersection of said first scribe line and said second scribe line through said wafer support;

aligning a drilling device at said intersection; drilling through said wafer from said front-side surface to a back-side surface of said wafer at said intersection with said drilling device to form an alignment mark on said back-side surface of said wafer;

aligning a saw with said first scribe line using said alignment mark; and

cutting said wafer from said back-side surface with said saw along said first scribe line, wherein said wafer support protects said front-side surface during said cutting. (Emphasis added.)

For reasons similar to those discussed above, Claim 21 is allowable over Wojnarowski in view of Roberts Jr., et al.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

7) Claims 3-6 and 14-21 are patentable over Wojnarowski in view of Summerer.

Claim 2 has been canceled thus obviating the rejection of Claim 2.

At page 4 of the Office Action, the Examiner admits that:

Wojnarowsky fail to teach coupling a front-side surface of a wafer to an interior surface of a transparent wafer support; ... (emphasis added.)

The Examiner cites Summerer as teaching:

... Summerer (Fig. 1) in a related method for alignment of substrates teaches shining light of an angle to a surface of a substrate (12) to detect alignment marks ... (Office Action, page 5.)

However, this does not cure the glaring deficiency of Wojnarowski noted above. Accordingly, Claims 3-6, 14-21 are allowable over Wojnarowski in view of Summerer.

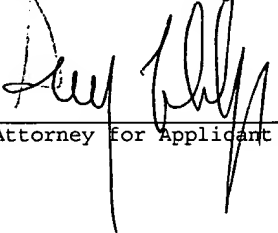
For at least the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Claims 1, 3-21 are pending in the application. For the above reasons, Applicants respectfully request that a timely Notice of allowance be issued in this case. If the Examiner has any questions relating to the above, the Examiner is requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF MAILING

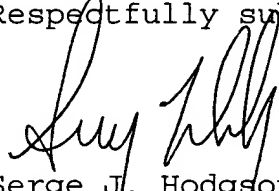
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 3, 2003.



Attorney for Applicant(s)

July 3, 2003
Date of Signature

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